智慧半導體奈米系統技術研究中心

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2020 年智慧半導體奈米系統技術研究中心
線上研究成果發表會

會議手冊

線上會議(Oral presentation) 日期: 11 月 25~26 日

Zoom 會議 ID: 315 567 3615　會議密碼:545616

(請於會議開始 3 分鐘前登入)

額外 MP4 papers 成果展覽網址:https://cstr.nctu.edu.tw

總主持人: 胡正明 院士

本中心致力於發展新穎之半導體技術，協助產業克服技術瓶頸。歡迎學研界共襄盛舉，參與本中心成果發表會!

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2020 年智慧半導體奈米系統技術研究中心
線上研究成果發表會議程

No.	Nov. 25,	Title
0	10:30~10:40	Opening (胡正明 院士)
1	10:40~11:20	Crystal-Orientation-Tolerant Voltage Regulator using Monolithic 3D BEOL FinFETs in Single-Crystal Islands for On-Chip Power Delivery Network (黃柏蒼教授)
2	11:20~12:00	STM Characterizations of 2D Materials and Devices (林俊良教授)
3	12:00~12:30	Understanding the ferroelectric Hf0.5Zr0.5O2 formation based on kinetic model (張書睿 助理研究員)
4	13:30~14:00	Phase Diagram of HZO on TiN Substrates - First-Principles Study (陳韻文博士)
5	14:00~14:30	Two Strategies for Decreasing Contact Resistance Between TMD and Metal Leads: A First Principles Study(林耿民博士)
6	14:30~15:00	Interface Engineering of ALD AlN on WS2 FETs (王信淵)
7	15:00~15:30	First-principles Quantum-transport Calculations of TMD/Metal Contact (楊琮甫)
8	15:30~16:00	Optimizing the Thermal Stability of Ultrathin GeOx Films by Ti Doping (Pratyay Amrit)
	16:00~17:00	Live Q/A with additional MP4 papers authors (#1~#9)
No.	**Nov.26**	**Title**
9	10:30~11:00	Steep subthreshold-swing InGaAs FETs Using Ferroelectric Materials (柯驊倫)
10	11:00~11:30	Exploring the High Mobility Performance via Gate-Dielectric Engineering of MoS2 Channel (塗浩瑋)
11	11:30~12:00	Enhancement on the bonding strength of Cu-Cu joints by 2-step annealing. (王家俊)
12	12:00~12:30	Impacts of Nitridation on Ferroelectric HfZrO2 Crystal Structures (林逸然)
13	13:30~14:00	Metal Electrode-induced Phase Uniformity on $Hf_{0.5}Z_{r0.5}O_2$ Thin Film (鄧智宇)
14	14:00~14:30	Phase Transformation of the Hf0.5Zr0.5O2 Affected by Pulse Electric Field During Thermal Annealing (鄭佳杰)
15	14:30~15:00	Single-Crystal-Islands Technique of Si for Monolithic 3D BEOL FinFET Circuits (鍾昊東)
16	15:00~15:30	Visualizing Self-Recovery of PtTe2 Surfaces (陳琬忻)
17	15:30~16:00	S-curve Engineering for ON-state Performance using Anti-ferroelectric/Ferroelectric Stack Negative-Capacitance FinFET (黃士恩)
	16:00~17:00	Live Q/A with additional MP4 papers authors (#10~#18)

Crystal-Orientation-Tolerant Voltage Regulator using Monolithic 3D BEOL FinFETs in Single-Crystal Islands for On-Chip Power Delivery Network

Po-Tsang Huang[1*], Yu-Wei Liu[1], Kuan-Fu Lai[1], Yun-Ping Lan[1], Tzung-Han Tsai[1], Bo-Jheng Shih[1], Ping-Yi Hsieh[2], Chih-Chao Yang[2], Chang-Hong Shen[2], Jia-Min Shieh[2], Da-Chiang Chang[2], Kuan-Neng Chen[1], Wen-Kuan Yeh[2], and Chenming Hu[1,3]

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Abstract

A single-crystal-island (SCI) technique is demonstrated using low thermal budget pulse laser process to fabricate single-crystal islands for monolithic 3D back-end-of-line (BEOL) FinFET circuits. The grain-boundary free Si FinFETs thus fabricated exhibit steep sub-threshold swing (<70mV/dec.), high driving currents (n-type: 363 μA/μm and p-type: 385 μA/μm), and high I_{on}/I_{off} (>10^6). According to simulation, the thickness of the interlayer dielectric plays an important role and shall be thicker than 250nm so that the sequential pulse laser crystallization process does not heat the bottom devices and interconnects to more than 400 °C. The single-crystallinity are verified with SECCO etch, HREM, TEM, and EBSD. BEOL FinFETs fabricated in the designed single-crystal Si islands exhibit excellent electrical performance and low intra-island variability. To mitigate the effects of island-to-island device variation due to random island crystal orientations, crystal -orientation-tolerant voltage regulator is further proposed by allocating power gating (PG) cells among multiple Si islands, and 42% power noise suppression can be achieved.

11:20~12:00

STM Characterization of 2D Materials and Devices

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Abstract

Current semiconductor industry is facing a limit of scaling. Thus, it is urgent to find a new type of material to replace Si. Two-dimensional (2D) materials, especially those with a proper band gap provide a solution to this problem since the thickness of a monolayer of 2D materials can be reduced to only few atoms. Scanning tunneling microscopy (STM) is a powerful method to reveal both the geometry and electronic structure down to atomic scale. In this presentation, I will discuss several issues of 2D materials and devices studied by STM. First, the growth behavior of silicene, a monolayer honeycomb structure of Si, is clearly revealed. Second, the location of defect in monolayer transition metal dichalcogenides (TMDs) is clearly identified though the quasiparticle interference. Besides, to recover the imperfect TMD surfaces is realized through in situ sputtering and annealing. Finally, the defect induced mobility modulation in 2D devices is visualized by STM. It is clear that STM can provide vital information for helping the developments of 2D materials and devices.

12:00~12:30

Understanding The Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ formation Based on Kinetic Model

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Abstract

$Hf_{1-x}Zr_xO_2$ (HZO) is a kind of ferroelectric (FE) material that holds promise for transistors and non-volatile memory due to great compatibility to CMOS technology. Although current studies support the importance of this material, the efficiency of ferroelectric formation limits HZO towards being fully engaged to the desired technologies. In this study, the kinetic model would predict the phase formation and phase transition of HZO film which has three phases of the orthorhombic (*O*), tetragonal (*T*) and monoclinic (*M*) phases. It is able to predict the condition of crystallization and phase transition during the thermal rapid and cooling process that govern ferroelectricity in HZO thin film. Our simulation reveal that the comparable interfacial energy between capping electrode and HZO would suppress the *M*-phase formation and enable more phase transition from *T*- to *O*-phase. By incorporating the kinetic model into the results from XAS mapping technique, we propose a soak annealing process to optimize the ferroelectric HZO. The process enabled HZO with a polarization (P_s) value up 64.52 μC cm^{-2}, which is the largest P_s ever reported in HZO system. The significant ferroelectric enhancement with soak annealing is due to the effective $T \rightarrow O$ phase transition along with the *M*-phase suppression.

13:30~14:00

Phase Diagram of HZO on TiN Substrates – First-Principles Study

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Abstract

HfxZr1-xO2 (HZO) is widely applied in many electronic devices for its high-κ property and also good compatibility in silicon based semiconductor manufacture. Recently, the accidentally found ferroelectricity in Si-doped HfO_2 (Si:HfO_2) opens new avenues of using doped HfO_2 and HZO related materials in negative capacitance, Fe-RAM, Fe-FET, energy storage, and etc. The formation of orthorhombic $Pca2_1$ phase in doped HfO_2/HZO thin film is recognized to be the origin of strong ferroelectricity. Years of experimental and theoretical studies found that conditions of doping, defects, substrates, annealing temperature, wake-up procedure and other factors during fabrication process will affect the population of orthorhombic $Pca2_1$ phase in thin film. The studies on fabricating doped HfO_2/HZO thin film with high population of orthorhombic phase are still ongoing. In this study, we investigated the effects of different HZO/TiN interfaces on the phase population of HZO thin film. Three most observed phases (monoclinic ($P2_1/c$), orthorhombic ($Pca2_1$), and tetragonal ($P4_2/nmc$)) were considered. The surface energies of HZO/TiN interfaces were calculated at the level of first-principles. With the aid of free energy model for thin film [1,2], we sketch the phase diagrams of HZO(111)/TiN(110) and HZO(001)/TiN(001) interfaces with considering the dependences on grain size, thin film thickness, and temperature. It is found that the population of orthorhombic phase would increase for thinner film, which is consistent with experimental observations. However the HZO(001)/TiN(001) interface would have much higher population of orthorhombic phase than HZO(111)/TiN(110) interface with the same film thickness.

[1] C. Künneth, R. Materlik, and A. Kersch, J. Apply. Phys. **121**, 205304 (2017).

[2] Y.-B. Tang et al., 2019 Symposium on VLSI Technology, Kyoto, Japan, 2019 pp. T22-23.

14:00~14:30

Two Strategies to Reduce Contact Resistance between TMDs and Leads: A First Principles Study

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Abstract

Monolayer transition-metal dichalcogenide (TMD) semiconductors are considered candidates for channel materials in next-generation transistors because of their suitable band gaps and high mobilities. However, a high contact resistance between TMDs and conventional metal leads limits the application of the TMDS devices. Some theoretical strategies have been studied to reduce contact resistance and confirmed by Schottky barrier and charge density distribution between channel and leads. Nevertheless, few theoretical researches evaluate the contact resistance by the relation between bias voltage and current density. Furthermore, the current density of industry criterial is 500 micro-Ampere per micro-meter with applying bias voltage 50 millivolts. We suggest two strategies. The T-phase of TMD as a buffer layers or adding halogen atoms between TMDs and metal leads. The phase engineering of two-dimensional TMDs has been studied recently, the phase transition is achieved by several methods. The T phase of monolayer $MoSe_2$ is a semimetal, in contract, the H phase of it is a semiconductor with the band gap 1.7 eV. Meanwhile, the doped halogen atoms may increase carrier density near the fermi level. The quantum transport was applied because the mean free path of an electron is shorter than the length of the channel. The constrained structure relaxation and the electronic structures are executed within the frame work of the DFT. Quantum transport properties were calculated in the frame work of the DFT method, combined with the NEGF as implemented in the Nanodcal package. It calculates the transmission coefficient between two leads. The Landauer's formula is used to calculate the current which is obtained from the transmission coefficient without applying bias and gate voltages. We used a short channel to get the contact resistance in order to exclude a resistance of the semiconductor channel. Our strategy can satisfy the industry's criterial.

14:30~15:00

Interface Engineering of ALD AlN on WS_2 FETs

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Abstract

For the development of advance two-dimensional (2D) electronic devices, the high-quality high-κ dielectric on 2D materials is essential. However, the growth mechanism on 2D materials by atomic layer deposition (ALD) has not been fully investigated. In this work, the 2D AlN interfacial layer on WS_2 was successfully formed by ALD for the first time. The 250 ℃ plasma-enhanced ALD (PEALD) 2D AlN on WS_2 demonstrates the feasibility of using low temperature ALD process to deposit high-κ dielectric directly on transition metal dichalcogenide (TMD) material. Comparing to h-BN, 2D-AlN is more suitable for IC fabrication process due to the low process temperature. The key is lattice matching between the TMD (WS_2) and the dielectric (AlN). Atomistic simulation reveals lower band distortion of WS_2 by 2D AlN interfacial layer (IL) than 2D h-BN IL, which has poorer lattice match with WS_2. The consequences are better transistor subthreshold swing and current drive. Experimental and theoretical results all indicate that the use of ALD 2D IL in TMD transistor gate stack is a promising step toward the development of future dense 3D IC.

15:00~15:30

First-principles Quantum-transport Calculations of TMD/Metal Contact

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Abstract

已知目前研究 TMD/Metal Contact 結構的模型主要分為:top, side, edge, C 等 4 種，其中後兩種屬於發揮 side-contact 優點的衍生型，如圖(1)。由於 top-contact 因受制於凡德瓦間隙(vdW-gap)之影響、導致 TMD/Metal 介面接觸電阻增加。而 side-contact 則因側面接觸 TMD、所以不會有來自 TMD 垂直面之 vdW-gap 的影響，故可使金屬電極(Lead $_{Metal}$)與 TMD 中間的金屬(TMD $_{Metal}$) 兩者原子接觸間距縮小，使裸露於 TMD 側截面的 TMD $_{Metal}$ 與 Lead $_{Metal}$ 較容易產生金屬鍵結，故而大幅降低接觸電阻。因此本研究重點將放在 side-contact 為主來進行研究，我們選擇 4 種 TMD 材料如：WS_2, WSe_2, MoS_2 及 $MoSe_2$ 作為通道材料，與 5 種 Lead $_{Metal}$ 如: Pt, Al, Ti, Au, Cu 結合之 side-contact 模型。透過第一原理的 DFT 方法，使用 VASP 軟件包來進行結構優化(relax)，與晶格匹配分析，各種金屬電極經模擬計算後皆選擇晶格匹配度最低的 FCC(面心立方)之 110 晶向來與 TMD 建模，如圖(2-b)。最後使用非平衡格林函數(NEGF)量子傳輸之 nanodcal 軟件包計算各種 TMD/Metal 之 side-contact 模型的 IV 曲線。

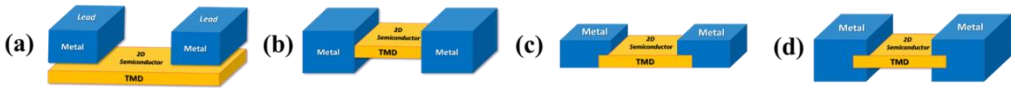

FIG.1 (a) top-contact, (b) side-contact, (c) edge-contact, (d) C-contact .

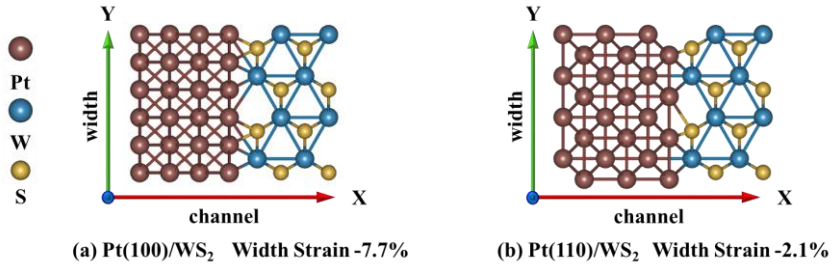

FIG.2, Pt/WS_2 在 Side-contact 中 Pt 金屬的兩種晶格匹配度 (a) Pt(100)/WS_2 strain -7.7% (b) Pt(110)/WS_2 strain -2.0%，很明顯 Pt(110)之晶格匹配較不失真。

15:30~16:00

Optimizing the Thermal Stability of Ultrathin GeOx Films by Ti Doping

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Abstract

Thermal stability of the dielectric interfacial layer inside the metal-oxide-semiconductor field-effect transistor (MOSFET) can affect the quality of the final products during the fabrication process of post metallization annealing, especially when the dielectric interfacial layer thickness is reduced to sub-nanometer. One vital problem is whether the size and location of the band gap might be changed by the annealing treatment. Here, we provide a direct measurement of band gap by scanning tunneling spectroscopy (STS) together with the valence band edge determined by ultraviolet photoemission spectroscopy (UPS). The band gap of the ultrathin GeO_x film (about 0.7 nm) grown on Ge substrates by atomic layer deposition (ALD) is clearly revealed. STS spectra show that the band gap of the GeO_x film is significantly modified after the annealing treatment. Meanwhile, UPS spectra also confirm the shift of the valence band edge. The pristine ultrathin GeO_x film behaves sensitive to the annealing treatment. However, for the GeO_x film with Ti doping, the band gap of the film becomes robust to the annealing treatment. Both the band gap and the valence band edge remain unchanged after the annealing treatment. It means that a small amount of Ti can enhance the thermal stability of the ultrathin GeO_x film.

10:30~11:00

Steep subthreshold-swing InGaAs FETs Using Ferroelectric Materials

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Abstract

Since the ultra-scaled MOSFET devices are reaching their fundamental physical limitation of the k_BT/q subthreshold swing (SS), the negative capacitance (NC) concept has emerged as one of promising solutions to overcome the Boltzmann tyranny. The NC effect has been realized by using various ferroelectric (FE) materials in the gate dielectric of the transistors. Among many FE materials, $HfZrO_x$ (HZO) thin films deposited by ALD have been introduced in both planar and non-planar NC FETs with SS below 60 mV/dec at room temperature. Steep SS properties are reported on Si, Ge, and GeSn FETs featuring FE HZO gate stack for the future lower voltage FET operations. InGaAs materials, owing to its extremely high carrier transport properties, have been widely investigated as the alternative channel materials in the electronic devices. However, not much study has been done on the demonstration of NC effect on InGaAs MOSFETs. A high density of interface trap states in the InGaAs MOS structures can be the root, prohibiting the NC behaviors to be achieved in the MOSFETs. In this article, the electrical properties of NC InGaAs MOSFETs with different HZO thicknesses are studied. Moreover, for the first time, the NC InGaAs FinFETs with sub-k_BT/q SS are fabricated and characterized.

11:00~11:30

Exploring the High Mobility Performance via Gate-Dielectric Engineering of MoS_2 Channel

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Abstract

Two-dimensional (2D) material such as graphene, MoS2, and h-BN etc, attracting lots of attention in recent years. In previous researches, the 2D material not only applies in switching devices as field-effect transistors (FETs) but also shows the high potential for logical, optical and bio-sensor applications. However, it is a challenge to substitute the 2D material as a silicon, which employing the 2D material as a channel suffers the trapped charge from the oxide layer easily. The h-BN as dielectric layer which can block the charge impurity from SiO2 and forming a MoS2 /h-BN heterostructure to fabricate the 2D-FET device. The dielectric constant of h-BN is 4 which is similar with SiO2 as a good insulating layer. Compare with SiO2, h-BN has atomic flat surface and free dangling interface which show the good performance in dielectric engineering of FETs device.

In this work, the h-BN as dielectric material showing low characteristic temperature (T0), which not only reducing the scattering form SiO2 substrate but also screening the doping effect from substrate. Also, the contact problem of MoS2 /h-BN shows the low contact resistivity and lower Schottky barrier height. Furthermore, we also utilize the h-BN as top gate dielectric layer todemonstrate double gate FET device. Compare with single gate device, the double gate can improve the subthreshold swing (SS.), current density (Jon) and mobility.

11:30~12:00

Enhancement on the bonding strength of instantly-bonded Cu-Cu joints by post annealing

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Abstract

This study investigates the bonding time and temperature on shear strength in copper-to-copper direct bonding with highly <111> oriented nanotwinned copper. Instant bonding process was performed under 10 and 30 seconds and post-bonding annealing was executed at 300 °C. Before bonding process, we use CMP to polish the surface of microbumps to reduce surface roughness.

The advantage of the two steps bonding is that we can obtain enough bonding strength in extremely short time due to very large diffusivity of our highly <111> oriented nanotwinned copper in the first step bonding process. We further more increase the bonding strength of the samples by the second-step annealing process by grain growth. By now, we successfully to fabricate the sample with only first bonding step process in 10 seconds and the shear strength can reach to 55MPa and the bonding strength can increase to above 110MPa after 300 °C/150 N post bonding annealing in one hour.

12:00~12:30

Impacts of Nitridation on Ferroelectric $HfZrO_2$ Crystal Structures

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Abstract

In this work, we present preliminary results on N incorporation into $Hf_{0.5}Zr_{0.5}O_2$ (HZO) using remote NH_3 plasma treatment on the top metal-oxide-semiconductor (MOS) capacitor. The indirect plasma treatment was used to change the bonding of HZO and favors no damages on the thin-films. Synchrotron radiation x-ray techniques provide a high-resolution spectrum for microstructures. X-ray diffraction (XRD) suggests that the crystallinity of HZO thin films varies with plasma treatment significantly. In addition, the deeper signals of structure can be detected by hard x-ray photoelectron spectroscopy (HAXPES). The information of electrical properties of HZO was studied by polarization – voltage (PV) loop.

13:30~14:00

Metal Electrode-induced Phase Uniformity on $Hf_{0.5}Zr_{0.5}O_2$ Thin Film

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Abstract

High-*k* gate oxides like $Hf_xZr_{1-x}O_2$ (HZO) have been the workhorse for the semiconductor industry in the last decades. The compatible fabrication process to MOSFET and room temperature ferroelectricity make HZO a long-time candidate for the high-*k* dielectric in NCFET. In the course of HZO development, it was found that for thin layers in the range of several nano-meters the ferroelectric phase becomes delicate. Phase determination in HZO used to rely on cross-comparison between x-ray diffraction (XRD) and polarization-electric (*P*-*E*) measurements. In this work, we develop a methodology for determining phase homogeneity and quantification based on X-ray absorption fine structure (XAFS). We established theoretical XAFS spectra of possible phases separately. By choosing different incident energy and scanning, the fluorescence on each spatial point can be detected. Through modified linear combination fitting, the phase composition can be obtained. Based on XAS mapping result, the ferroelectric property can be tuned by capping electrodes, TiN/TaN/Mo. The scanning phase composition shows good match to the P-E loops and XRD results. In conclusion, this method served a powerful way for probing phase homogeneity of HZO. Spatial mapping of the phase distribution would facilitate the device optimization as it establishes a bridge correlating HZO's microscopic and macroscopic properties.

14:00~14:30

Phase transformation of the $Hf_{0.5}Zr_{0.5}O_2$ induced by pulse electric field during thermal annealing

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Abstract

High-k gate oxides have been the workhorse for the semiconductor industry in the last decades. Device scaling is one of the most important factors, while the film quality, taking $Hf_{1-x}Zr_xO_2$ (HZO) as an example, is often sacrificed during thickness reduction due to phase instability. Enhancement of phase uniformity of ALD-grown HZO requires (i) powerful analytical tools that can probe the chemical state and crystal ordering of the film, and (ii) new optimization processes based upon the understanding of the analysis.

We adopted an electric-pulse assisted (EPA) process during thermal annealing to optimize the HZO films. The EPA provides a degree of freedom to control charged vacancy by electrically stressing the film during annealing. As reported, the migration of oxygen vacancies plays an important role in film nucleation[1], and phase uniformity might be improved if the EPA is properly applied. We used synchrotron x-rays to conduct interface characterizations, with emphasis on exploring the (i) inter-relation between film's oxygen state and capping electrodes and (ii) phase transformation, while applying the EPA. The microscopic and macroscopic properties of the HZO were correlated by linking the synchrotron and the polarization-voltage (P-V) results. We present preliminary results of x-ray diffraction patterns versus EPA treatments. We obtained significant relocation of the peaks upon different EPA stressing voltages. It can be interpreted as the phase transition arising from the migration of oxygen vacancy. More characterizations such as x-ray photoelectron spectroscopy (XPS), is needed to further understand the interface reconstruction.

Reference: [1] Zhou, Y , et al. Comput. Mater. Sci. **167**, 143-150, (2019).

Single-Crystal-Islands Technique of Si for Monolithic 3D BEOL FinFET Circuits

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Abstract

As Moore's law proceeding, the scaling of transistors reached to its physics limits. The concept of monolithic 3D ICs thereby attained more and more interest and was considered to be a convincing technique. In this study, a single-crystal-islands (SCI) technique was demonstrated using low thermal budget pulse laser process to fabricate single-crystal silicon islands for monolithic 3-D back-end-of-line (BEOL) FinFET circuits. The lithography-defined silicon islands were placed on cooling holes and encapsulated in comformal silicon nitride films. By laser recrystallizing those, the single-crystal Si islands would be obtained. The crystallinity of Si islands was first verified with SECCO Etch, HREM, TEM, and EBSD. Furthermore, the BEOL FinFETs in SCI Si islands were following fabricated to certify their performance. Thanks to the single-crystalline Si islands free from grain boundary degradation, the FinFETs in SCI Si islands exhibited better average on current (I_{ON}) of 311.73 μA/μm and lower intra-device variability than the ones in poly-Si. Therefore, the fabrication of FinFETs in SCI technique would be a promising art for monolithic 3D BEOL FinFET circuits.

15:00~15:30

Visualizing Self-Recovery of $PtTe_2$ Surfaces

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Abstract

In the past decade, layered materials stacked by Van der Waal interaction create a large number of fascinating researches. Transition metal dichalcogenides (TMDs) with huge diversities share remarkable properties in many fields [1]. They exhibit an extremely high potential for next-generation devices from electronics to optics. $PtTe_2$ is also a typical TMD materials crystallizing in 1T structure. Recently, a layer-dependent semiconductor-semimetal transition has been reported for $PtTe_2$[2], which increases its application possibility. By scanning tunneling microscopy (STM), we found CVD-growth $PtTe_2$ surface with many intrinsic defects after *in situ* cleavage. It can self-recover after sputtering and annealing process. This result provides us a new method to manufacture defect-free TMD layers.

Keywords: Transition Metal Dichalcogenides (TMDs), Platina Ditelluride ($PtTe_2$), Defect, Scanning Tunneling Microscopy (STM)

Reference:

[1] C. L. Lin et al., J. Phys.: Condens. Matter **32** 243001 (2020).

[2] M. K. Lin et al., Phys. Rev. Lett. **124**, 036402 (2020).

15:30~16:00

S-curve engineering for ON-state performance using anti-ferroelectric/ferroelectric stack negative-capacitance FinFET

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Abstract

This work investigates the S-curve engineering by exploiting the anti-ferroelectric (AFE)/ferroelectric (FE) stack negative-capacitance FinFET (NC-FinFET) to improve both the subthreshold swing and ON-state current (I_{ON}). Our study indicates that the AFE/FE gate-stack can theoretically achieve surprising improvements to the OFF-state current (I_{OFF}) and I_{ON} relative to IRDS projections. There is significant long-term advantage to IC power consumption and speed if materials with certain AFE and FE characteristics can be developed and introduced into IC manufacturing.