

High-Accuracy Deep Neural Networks Using a Contralateral-Gated Analog Synapse Composed of Ultrathin MoS₂ nFET and Nonvolatile Charge-Trap Memory

Yunyan Chung

Department of Electronics Engineering and the Institute of Electronics,
National Chiao Tung University, Hsinchu, Taiwan

sniper.ee05g@g2.nctu.edu.tw

Abstract

The development of high-accuracy analog synapse deep neural networks entails devising novel materials and innovative memory structures. We demonstrated an analog synapse with contralateral gates based on a two-dimensional (2D) field-effect transistor and nonvolatile charge-trap memory. Vertical integration of a MoS₂-channel FET with a charge-trapping layer provided excellent charge controllability and gate-tunable nonvolatile storage. In the proposed contralateral-gate design, the read and write operations were separated to mitigate read disturb degradation. Reducing the MoS₂ channel thickness to the ultrathin scale allowed large threshold voltage shifts and on-resistance (R_{ON}) modulations. This vertically integrated MoS₂ synapse device exhibited 55 conductance states, high conductance max–min ratio (G_{MAX}/G_{MIN} ; ~50), low nonlinearity of $\alpha_p = -0.81$ and $\alpha_d = -0.31$, near ideal asymmetry of 0.5, and free of read disturb degradation. High neural network accuracy (>87%) is also obtained.