Title: Location-Controlled-Grain Technique with Novel Cooling Hole Structure for Monolithic 3D BEOL FinFET Circuits

Yu-Wei Liu[1], Yi-Jui Chang[1], Chih-Chao Yang[2], Chang-Hong Shen[2], and Kuan-Neng Chen[1], and Chenming Hu[1,3]

1National Chiao Tung University, Hsinchu, Taiwan, 2Taiwan Semiconductor Research Institute, Hsinchu, Taiwan, 3Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA, USA

1*E-mail: knchen@mail.nctu.edu.tw; 1,3**E-mail: hu@eecs.berkeley.edu

Abstract

In this study, the quality of silicon channel fabricated by cooling hole structures is investigated, including different structures and kinds of dielectric layers. The discontinuous dielectric layer of Si3N4 can assist to provide high-quality silicon channel due to the induced thermal stress. Based on the high-quality result of silicon channel, location-controlled-grain technique with a discontinuous layer of Si3N4 could be a feasible technology and scheme to achieve high performance monolithic 3D integration circuits. LCG technique has been successfully demonstrated. By using the cooling hole structure with the discontinuous dielectric layer of Si3N4, high-quality silicon channel was obtained and the electrical properties of FinFETs fabricated with this scheme were further improved. Thus, this improved scheme can provide a high-quality silicon channel and accordingly realize monolithic 3DIC.

The cooling hole structure can provide high quality polycrystalline silicon channel in location controlled grains. In addition, the crystallinity of silicon channel can be further improved by adopting the symmetrical cooling hole shape.The cooling hole structure can allow only one grain filtered out and show better crystallinity after secco etching. Moreover, the symmetrical shapes of the cooling hole can provide silicon channel with better quality than other shapes do. Accordingly, with this LCG technique, the grain boundary effect induced from random grains can be effectively removed.