Simulation and Thermal Analysis of Location-Controlled-Grain Ge Technique for Monolithic 3DIC

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Abstract

For the past years, the size of electronic devices has scaled down to keep up with Moore's law. However, drawbacks of physical limitation and high cost of lithography tools for two-dimensional integrated circuits appear when Moore's law is in pursued. The monolithic 3D integration technique has been gradually emphasized because it could provide efficient connectivity of circuits, decrease power consumption, enhance system performance, and reduce chip size. In this research, we simulate the Location Control Grain (LCG) structure with Si and with Ge to investigate the monolithic 3DIC technique. In addition, the LCG structure with Ge under laser heating from 4W to 5.5W has been simulated. Finally, we compared the LCG structure with 150nm Ge layer and the LCG structure with 200nm Ge layer.