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## Phase Diagram of HZO on TiN Substrates – First-Principles Study

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### Abstract

$\text{Hf}_x\text{Zr}_{1-x}\text{O}_2$  (HZO) is widely applied in many electronic devices for its high- $\kappa$  property and also good compatibility in silicon based semiconductor manufacture. Recently, the accidentally found ferroelectricity in Si-doped  $\text{HfO}_2$  ( $\text{Si:HfO}_2$ ) opens new avenues of using doped  $\text{HfO}_2$  and HZO related materials in negative capacitance, Fe-RAM, Fe-FET, energy storage, and etc. The formation of orthorhombic  $\text{Pca}2_1$  phase in doped  $\text{HfO}_2$ /HZO thin film is recognized to be the origin of strong ferroelectricity. Years of experimental and theoretical studies found that conditions of doping, defects, substrates, annealing temperature, wake-up procedure and other factors during fabrication process will affect the population of orthorhombic  $\text{Pca}2_1$  phase in thin film. The studies on fabricating doped  $\text{HfO}_2$ /HZO thin film with high population of orthorhombic phase are still ongoing. In this study, we investigated the effects of different HZO/TiN interfaces on the phase population of HZO thin film. Three most observed phases (monoclinic ( $\text{P}2_1/\text{c}$ ), orthorhombic ( $\text{Pca}2_1$ ), and tetragonal ( $\text{P}4_2/\text{nmc}$ )) were considered. The surface energies of HZO/TiN interfaces were calculated at the level of first-principles. With the aid of free energy model for thin film [1,2], we sketch the phase diagrams of HZO(111)/TiN(110) and HZO(001)/TiN(001) interfaces with considering the dependences on grain size, thin film thickness, and temperature. It is found that the population of orthorhombic phase would increase for thinner film, which is consistent with experimental observations. However the HZO(001)/TiN(001) interface would have much higher population of orthorhombic phase than HZO(111)/TiN(110) interface with the same film thickness.

[1] C. Künneth, R. Materlik, and A. Kersch, J. Apply. Phys. **121**, 205304 (2017).

[2] Y.-Z. Tang et al., 2019 Symposium on VLSI Technology, Kyoto, Japan, 2019 pp. 121-123.